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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/845,896	TOWLE ET AL.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-18 and 24-45* is/are pending in the application.

4a) Of the above claim(s) *6* is/are withdrawn from consideration.

5)☒ Claim(s) *28-30 and 41-45* is/are allowed.

6)☒ Claim(s) *1-4,7-18,24-27,32,33,35,36,39 and 40* is/are rejected.

7)☒ Claim(s) *5,31,34,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *14*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/02/04 has been entered. An action on the RCE follows.

2. The amendment filed on 07/02/2004 has been entered.

Claim Objections

3. Claim 45 is objected to because of the following informalities:

Misnumbered claim 45 as recited in the amendment, page 11, line 4, should read, claim number "43".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 7-10, 18, 24, 27 and 36 are rejected under 35 U.S.C. 102(a) as being unpatentable over Brooks et al. (US Pat. 6084297).

Regarding claims 1 and 2, Brooks et al. disclose a microelectronic device package/electrical system (10 in Fig. 2) comprising:

- a die (14 in Fig. 1 and 2) having a top surface/active surface being fixed within an opening (see 54 in Fig. 2) in a package core (40/8 in Fig. 2), the package core being made of an adhesively coated frame/board-shaped dielectric material/insulating film having first insulating solder mask surface (8 in Fig. 2, Col. 6, line 1-34), the die being fixed by an encapsulation material (54 in Fig. 2) between the die and the package core
- a metallization layer built up upon said active surface of said die and the package core; the package core having a metallic layer/cladding of copper (50 in Fig. 2) at the top surface providing a ground/reference plane and improved rigidity and thermal dissipation (Col. 6, lines 35-45)
- a metallization layer built upon the die and the package core (36/22 in Fig. 2) the metallization layer having a first metallization portion located over the die (36 in Fig. 2) and a second metallization portion (22 in Fig. 2) located over the package core
- a grid array interposer unit/laminated substrate (16 in Fig. 2) laminated to the

metallization layer, the interposer having an array of electrical contacts/solder balls (26 in Fig. 2) on a second surface, and

- a carrier substrate/board (30 in Fig. 2) having a second array of electrical contacts/circuitry (28 in Fig. 2), the respective contacts of the interposer and the carrier substrate/board being conductively coupled through the solder balls

(Fig. 1 and 2; Col. 5, line 15- Col. 7, line 25).

Brooks et al. fail to explicitly teach a metallization layer built up on the active surface of the die.

Broooks et al. Further teach another embodiment (see Fig. 5), where the die is flip chip bonded such that the die has a first portion of a metallization on the active surface (see 46/126 on the die in Fig. 5) to provide the desired electrical connections on the active surface (Col. 8, lines 4-32).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metallization layer being built up on the active surface of the die as taught by the embodiment of Fig. 5 in Brooks et al. so that the desired electrical coupling and grounding can be achieved in Brooks et al's device.

Regarding claim 7, Brooks et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. disclose the package core having the

metallic layer/cladding of copper (50 in Fig. 2) at the top surface (Col. 6, lines 35-45).

Regarding claims 8-10, Brooks et al. teach substantially the entire claimed structure as applied to claims 1 and 7 above, and Brooks et al. further teach the metallic layer/cladding being coupled to ground, reference or power during operation of the device to provide the respective ground, reference or power plane/source for the wiring/transmission structure (Col. 6, lines 24-30; Col. 6, lines 45-48; Col. 7, lines 1-5) within the metallization layer through conductive vias, traces and conductive sites/pads (52/34, 32 and 44/24 respectively in Fig. 1 and 2) including the ground pad, the ground, reference or power connections being selected based on the application requirements (Col. 7, line 4).

Regarding claim 18, Brooks et al. teach substantially the entire claimed structure as applied to the claim 1 above, wherein the metallization between the die and the grid array interposer being a single metallization layer (36 in Fig. 2).

Regarding claims 24 and 36, Brooks et al. teach substantially the entire claimed structure as applied to the claim 1 above, wherein the electrical system comprises the die/core assembly having the substrate/circuit board (14/40 and 30 respectively in Fig. 1 and 2).

Regarding claim 27, Brooks et al. teach substantially the entire claimed structure as

applied to the claim 24 above, wherein the first array of electrical contacts include the plurality of solder balls (26 in Fig. 2).

6. Claims 3 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Kelly et al. (US Pat. 5798567).

Regarding claims 3 and 39, Brooks et al. teach substantially the entire claimed structure as applied to the claims 1 and 36 respectively above, except connecting at least one decoupling capacitor to the second surface of the grid array interposer unit to provide decoupling for the circuitry within the die.

Kelly et al. teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the grid array interposer/substrate to improve the electromagnetic interference (EMI) suppression and the electrical performance of the integrated circuit package (Col. 4, line 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one decoupling capacitor being connected to the second surface of the grid array interposer unit as taught by Kelly et al so that the EMI can be reduced and the desired decoupling for the circuitry can be achieved in Brooks et al's device.

7. Claims 4, 32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Sylvester (US Pat. 6014317).

Regarding claims 4 and 32, Brooks et al. teach substantially the entire claimed structure as applied to the claim 1 above, except the interposer having a thickness between the first and second surfaces being no greater than 0.5 mm.

Sylvester teaches using a grid array interposer unit/multilayered substrate (MLS 12 in Fig. 2) having the substrate thickness between the first and second surface such as about 2 mils, 3.9 mils, etc. (Col. 3, lines 10-15; Col. 24, line 5) to provide the desired stress reduction and surface irregularities (Col. 3, line 12), the thickness being no greater than 0.5 mm.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate except the interposer having a thickness between the first and second surfaces being no greater than 0.5 mm as taught by Sylvester so that the surface irregularities and the compressive stress can be reduced in Brooks et al's device.

Regarding claim 35, Brooks et al. and Sylvester teach substantially the entire claimed Structure as applied to claim 32 above, and Brooks et al. further teach the metallic layer/cladding being coupled to ground, reference or power during operation of the device to provide the respective ground, reference or power plane/source for the

wiring/transmission structure (Col. 6, lines 24-30; Col. 6, lines 45-48,. Col. 7, lines 1-5) within the metallization layer through conductive vias, traces and conductive sites/pads including the ground pad (52/34, 32 and 44/24 respectively in Fig. 1 and 2), the ground, reference or power connections being selected based on the application requirements (Col. 7, line 4).

8. Claims 11-17 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Harada et al. (US Pat. 5523622).

Regarding claims 11 and 12, Brooks et al. teach substantially the entire claimed structure as applied to claim 1 above, but fail to teach the active surface of the die including a plurality of power bars and ground bars distributed on the surface where each of the power and ground bars being conductively coupled to respective multiple power and ground pads of the die, power bars and ground bars being interleaved within a central region the surface of the die.

Harada et al. teach using a metallization pattern on a die where a plurality of power bars and ground bars are distributed on the surface and interleaved within a central region of the die where each of the power and ground bars (not numerically referenced in Fig. 1- see power and ground bar pattern in the central region) being conductively coupled to respective multiple power and ground pads (218d and 218e in Fig. 1 and 5) of the die (Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of power bars and ground bars distributed on the surface where each of the power and ground bars being conductively coupled to respective multiple power and ground pads of the die as taught by Harada et al so that the ground potential can be stabilized and the transmission characteristics can be improved in Brooks et al's device.

Regarding claim 13, Brooks et al. disclose substantially the entire claimed structure as applied to claims 1, and 11 above, except the die including a plurality of signal contact pads being distributed within a peripheral region of the active surface of the die.

Harada et al. teach using a metallization pattern on the die where a plurality of signal contact pads (218a, and 218b in Fig. 5) is distributed within central and peripheral regions of the surface of the die (Fig. 1 and 5., Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of signal contact pads being distributed within a peripheral region of the active surface of the die as taught by Harada et al. so that the transmission characteristics can be improved in Brooks et al's device.

Regarding claims 14 and 15, Brooks et al. disclose substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization layer including at least power or ground landing pad being situated over the die being

conductively coupled to multiple power or ground bond pads respectively through corresponding via connections.

Harada et al. teach using a metallization pattern on the die and the substrate where a power or a ground landing pad (not numerically referenced - see the power or ground landing pad situated above the via connecting the power layer 208 or ground layer 207 in Fig. 2) is conductively coupled to multiple power bond pads (218d in Fig. 5) through corresponding via connections (see vias 216 in Fig. 2, Col. 5, lines 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least power landing pad being conductively coupled to multiple power bond pads through corresponding via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Brooks et al's device.

Regarding claims 16, 17 and 40, Brooks et al. and Harada et al. teach substantially the entire claimed structure as applied to claims 1, 11, 13, 14 and 36 above, and Brooks et al. further teach the metallization layer including at least one ground, power or signal/I-O conductive site/landing pad (44 in Fig. 1 and 2) being situated over the package core and being conductively coupled to the respective multiple power or ground conductive site/bond pad on the die through the respective trace/transmission line portion (32 in Fig. 1 and 2) extending over the die and a plurality of via (34 in Fig. 1 and 2) connections (Col. 6, line 25- Col. 7, line 10).

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Taniguchi et al. (US Pat. 6388333).

Regarding claim 25, Brooks et al. teach substantially the entire claimed structure as applied to claim 24 above, except the circuit board being a computer motherboard.

Taniguchi et al. teach using a semiconductor mounting device/system having a variety of configurations including conventional substrates such as motherboard/computer motherboard (38 in Fig. 28, Col. 17, lines 30-35, Col. 11, lines 10-20).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a computer motherboard as the substrate as taught by Taniguchi et al. so that the desired mounting and external connection requirements can be achieved in Brooks et al's device.

10. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Blish, II et al (US Pat. 6049465).

Regarding claim 26, Brooks et al. teach substantially the entire claimed structure as applied to claim 24 above, except the first array of contacts including a plurality of pins.

Blish, II et al. teach using electrical contacts such as pins (150 in Fig. 1), balls, etc. to provide an external connection between the carrier/interposer and a PWB (Col.

1, line 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first array of contacts including a plurality of pins as taught by Blish, II et al. so that the integrity and reliability of the external connection can be improved in Brooks et al's device.

11. Claims 33 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) and Sylvester (US Pat. 6014317) as applied to claims 32 and 36 above, and further in view of Kelly et al. (US Pat. 5798567).

Regarding claims 33 and 39, Brooks et al. and Sylvester teach substantially the entire claimed structure as applied to the claims 32 and 36 above, except connecting at least one decoupling capacitor to the second surface of the grid array interposer unit to provide decoupling for the circuitry within the die.

Kelly et al. teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the substrate to improve the electromagnetic interference (EMI) suppression and the electrical performance of the integrated circuit package (Col. 4, lines 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to connect at least one decoupling capacitor to the second surface of the grid array interposer unit to provide decoupling for the circuitry within the die as

taught by Kelly et al. so that the EMI and thickness of the package can be reduced and the desired decoupling for the circuitry can be achieved in Sylvester and Brooks et al's device.

Allowable Subject Matter

12. A. Claims 28-30 and 41-45 are allowed.

B. Claims 5, 31, 34, 37 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

13. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "a die/core assembly having a microelectronic die fixed within an opening in a package core by an encapsulation material between said die and said package core, said die/core assembly having a first surface including an active surface of said die; a metallization layer built up over said first surface of said die/core assembly" and " a grid array interposer unit laminated to said metallization layer; and at least one capacitor conductively coupled to an exposed portion of said metallization layer" in a die/core assembly or "a die/core assembly including a die fixed within a package core, said die/core assembly having a continuous surface; a metallization layer built up upon said continuous surface; and a grid array interposer unit having a first

surface laminated to said metallization layer" in a die/core assembly having an interposer having external contacts for a connection to a circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

07-22-04

PATENT EXAMINER

TECHNOLOGY CENTER 2800